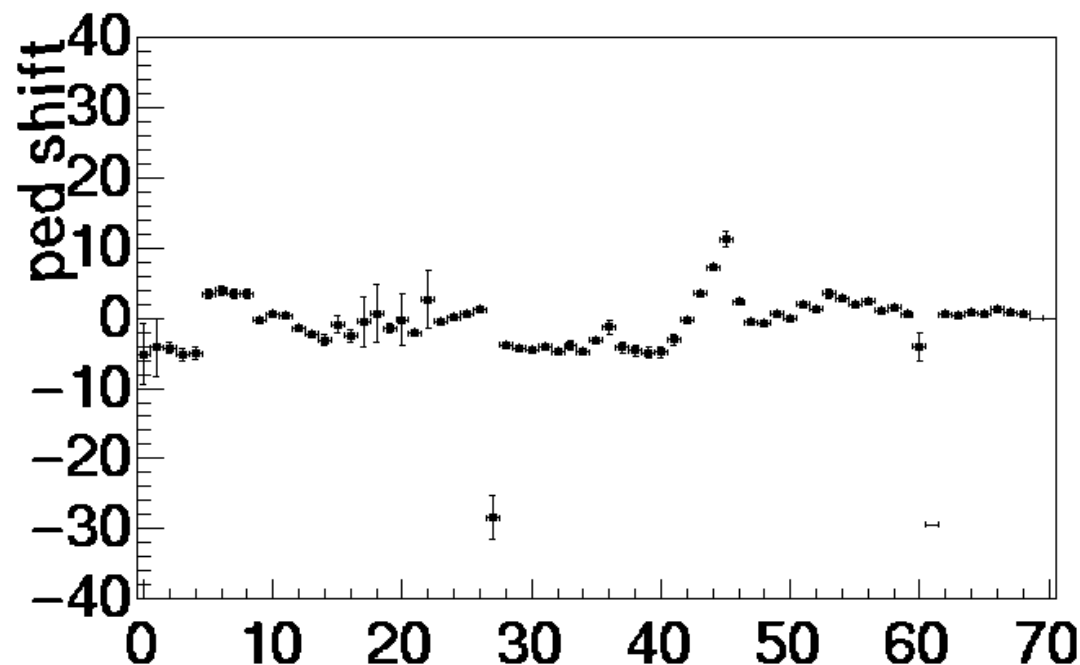# Pedestals vs. "Case Number"

In May, we (Glenn, Hubert, John) did a lot of tests on the MVD -- mainly looking at noise and pedestal shifts. See: http://www.phenix.bnl.gov/WWW/p/draft/sullivan/notes/mvd/may02_tests/ For one packet (neither the best nor the worst), here is a plot of the pedestal shift (compared to a randomly selected "standard" run) vs "case number":

# Packet 2031: Temperature dependence of pedestal position

Ped - "standard" ped
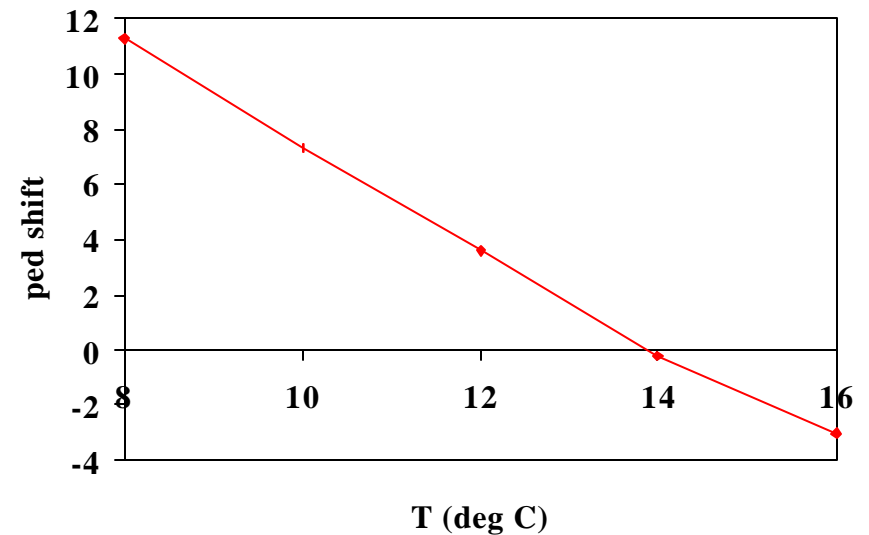
ped:index {ipack==2031 && index>25 && index<65}
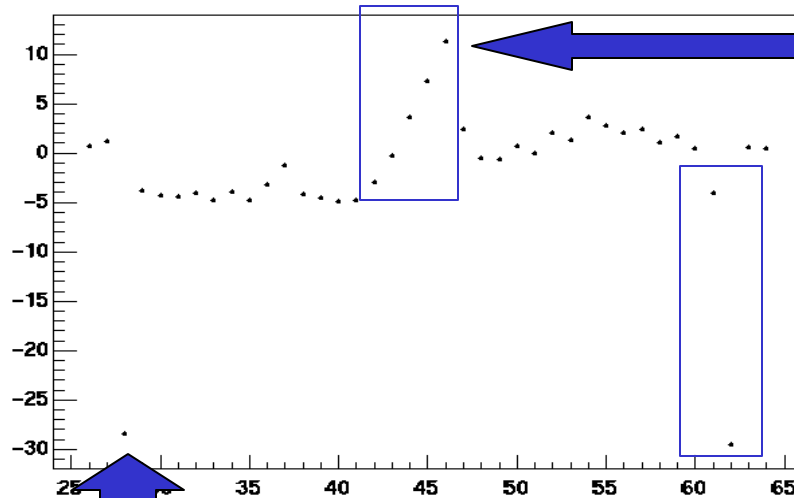
Ncase

Case 28,
Run 44006,
chiller not
working

Cases 61-62,
runs 44175-6,
fan+pump off

Chiller temperature reduced
in steps of 2 degrees from
16 to 8 degrees -- plot of
pedestal shift vs. temperature:

ped shift

T (deg C)

Slope ~ 1.78 chan/deg

# Temperature dependence

The chillers in our cooling system are (I think) set to allow to 2° fluctuations from the set point. However, I have never seen a working chiller more than a ~0.5° off.

Sigma of our pedestals is typically ~3 ADC channels. Zero-suppression cuts are at 2-sigma. So, 3-4° fluctuations would wreck our zero-suppression.

Could these be all or part of our pedestal shift problem? Observed T shifts say probably not.

Conclusion: We need to monitor and record data from the temperature sensors which are on each MCM.

# Omit runs with unusual Temp
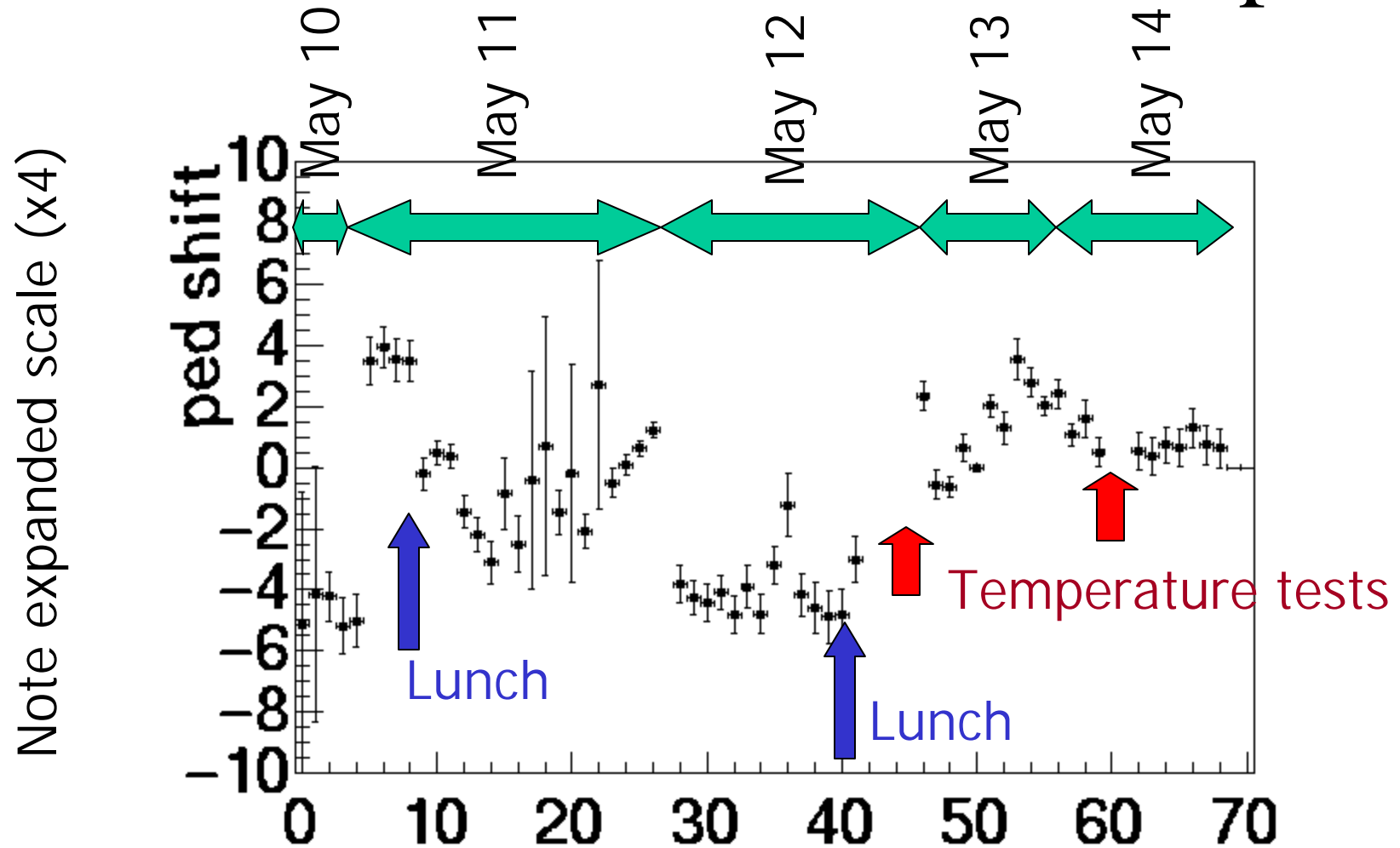


Most pedestal jumps came when we cycled power.

# MCM status - 1

The current MVD contains 81 MCMs out of 136 in the CDR design (60%) -- MCM yield and production schedule are the problems.

We ordered 4 more "lots" of 24 MCMs from Lockheed-Martin.

1 lot was delivered ~March
1 lot was delivered May 29
1 lot was delivered June 10
1 lot expected ~June 30

# MCM status - 2

Lot received in March had poor yield, of 24 MCMs:

4 rejected at Lockheed-Martin -- this number is typical.

7 have shorts in the surface mount components -- not typical, but has happened before and can usually be repaired.
We can't say whether these are "good" or "bad" yet.

11 were "bad" -- failed Q/A tests.

2 were "good" -- much worse than normal but not the first time we've seen such a poor yield.

# Summary/Plans

We have made some progress in understanding noise --
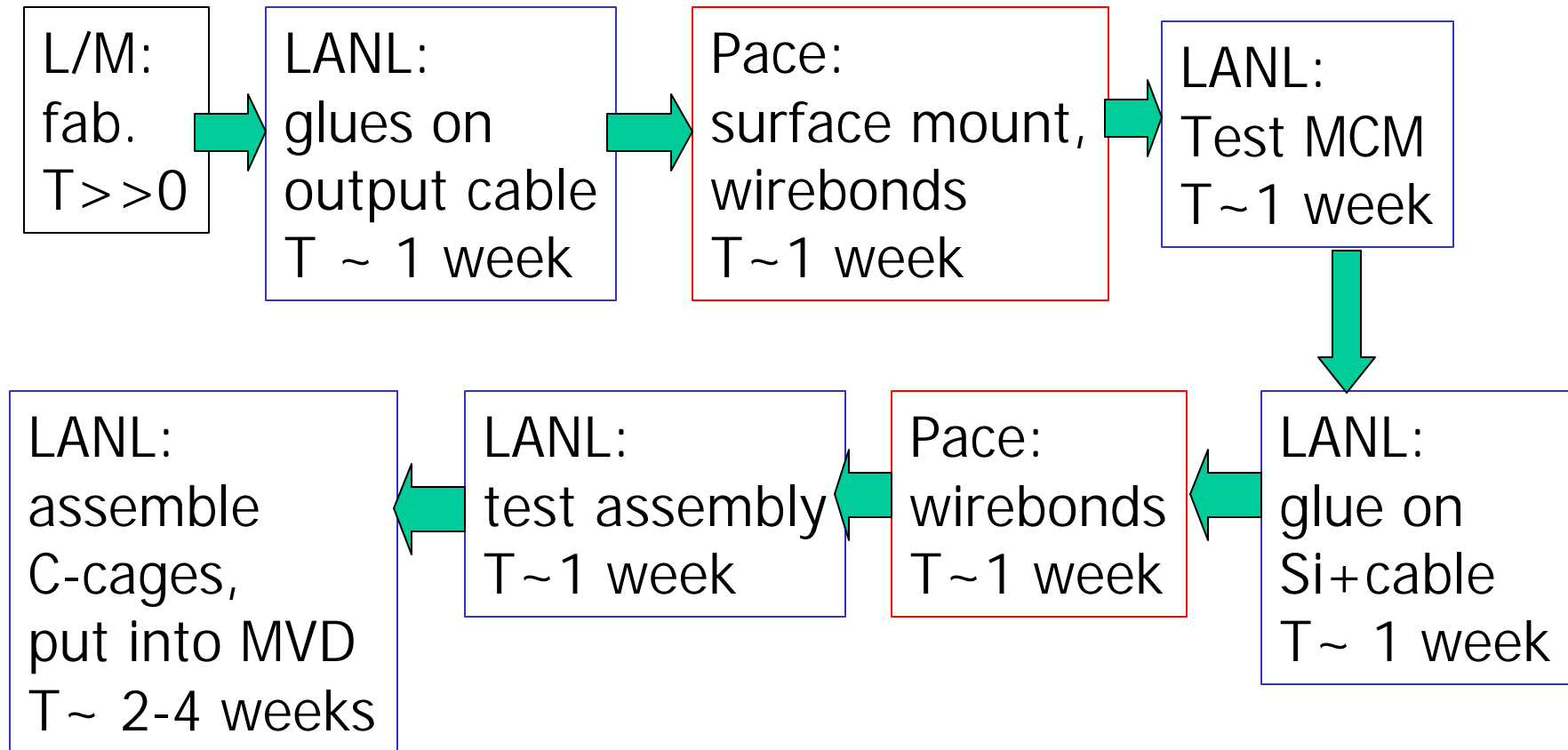one problem is deciding when it is better.

We see cross-talk between power/comm boards boards --
will try shielding

Glenn/Chuck/John/IhnJea will work next week.

Hubert/IhnJea working this week -- looking at FPGA codes

We need to look at FPGA codes more.

# The life cycle of an MCM lot

L/M:
fab.
T>>0

→

LANL:
glues on
output cable
T ~ 1 week

→

Pace:
surface mount,
wirebonds
T~1 week

→

LANL:
Test MCM
T~1 week

↓

LANL:
assemble
C-cages,
put into MVD
T~ 2-4 weeks

←

LANL:
test assembly
T~1 week

←

Pace:
wirebonds
T~1 week

←

LANL:
glue on
Si+cable
T~ 1 week

We currently have one lot in each of the first 3 steps and
one lot spread out over steps 3-5.